# **GENIE-XP**

# SAS-EXPANDER VERIFICATION IP

#### **OVERVIEW**

The Genie-XP Verification IP Product is the industry's most comprehensive verification solution for SAS based designs. Its intelligent **Verification Engine**, integrated **Interface Inspector** and comprehensive **Compliance Suite** provide the perfect combination of tools to ensure first silicon success.

The **Genie-XP VIP** provides a quick and efficient way to verify any SAS based design – Initiator, Expander or Target. It supports SAS 1.1, 2 and 2.1 specifications and tests all layers of the SAS protocol – Phy, Link, Port, Transport and Application. Genie-XP along with Genie-SAS Verification IP product provides a complete verification solution.

The Genie-XP VIP provides:

- Bus Functional Models
- Frame & Primitive Generator
- Error Injector
- Callbacks
- Monitor/Checker
- Report Generator

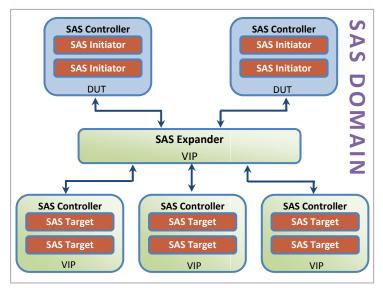


Fig 1: SAS Initiator Verification

# **FEATURES**

<ul> <li>Complete Functional SAS Verification - Initiators, Targets and Expander</li> </ul>	<ul> <li>Verification of all layers: Phy, Link, Port, Transport and Application</li> </ul>
SAS 1.1, 2 and 2.1 compliant	<ul> <li>System level and block level testing</li> </ul>
<ul> <li>Supports 1.5, 3.0 and 6.0 Gbps speeds</li> </ul>	<ul> <li>Full support for SSP, SMP and STP</li> </ul>
<ul> <li>Supports rate matching for both SAS and SATA connections</li> </ul>	<ul> <li>Number of Phys can be configurable from 2 to 128 Phys</li> </ul>
<ul> <li>Link Power management support</li> </ul>	❖ Wide Port & Narrow Port Support
<ul> <li>Configurable routing table and discovery pages</li> </ul>	<ul> <li>Protocol Checker – functionality at all layers</li> </ul>
<ul> <li>Supports SAS-SAS and SAS-SATA speed negotiation</li> </ul>	<ul> <li>Ability to integrate SATA Device into SAS domain</li> </ul>
<ul> <li>Scalable for multiple instantiations in a testbench to form all standard SAS topologies</li> </ul>	<ul> <li>Auto Discovery process feature allows to configure routing tables through test files</li> </ul>
<ul> <li>Configurable test generation for constrained random, directed and error testing</li> </ul>	<ul> <li>Ability to control and change packet value during transmission through each layer</li> </ul>
<ul> <li>Ability to enable or disable specific error checks and violations</li> </ul>	<ul> <li>Programmable parameters through configurable Knobs</li> </ul>
<ul> <li>User configurable reports for logging events and transactions</li> </ul>	<ul> <li>Multiple Language Interface – SystemVerilog, Verilog, VHDL, C/C++, SystemC, `e', VERA</li> </ul>
<ul> <li>Automatic and user configurable Callback capability</li> </ul>	









#### PRODUCT DETAILS

# **Phy Layer Features**

- Supports serial (1 bit) and parallel (10/20/40 bit) interface
- 8b/10b encoding and decoding
- Configurable OOB signals
- Phy multiplexing support
- Optional DC-IDLE pin
- Single or multi-bit error injection
- Automatic detection of SAS and SATA device connections

# **Link Layer Features**

- Support for all primitive sequences
- SAS Link Power Management support
- Ability to corrupt primitive sequence as well as transmit custom primitive sequences
- Ability to enable/disable scrambling on the fly
- Programmable Connection Rate independent of physical rate which enables rate matching without expander
- Applies Arbitration fairness rules
- Randomized or Directed error injection

### **Expander Function Features**

- Contains Expander Connection Manager (ECM), Expander Connection Router (ECR) and Broadcast Primitive Processor (BPP)
- User configurable routing tables and discovery pages
- Simultaneously manage multiple connections
- Follows ECM Arbitration requirements
- Programmable timers-arbitration wait, maximum connection timeout

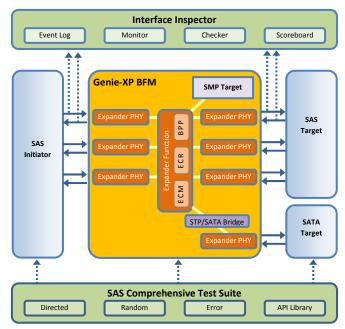


Fig 2: SAS Verification Environment

# **STP/SATA Bridge Features**

- Contains STP target port, SATA Host port and functions to bridge them
- Uses SATA link layer state machine in SATA Host port
- Supports all SATA primitives including HOLD, CONT.
- Supports Rate matching through ALIGN and HOLD primitives
- Follows all STP flow control rules
- Supports single affiliation policy

### SUPPORTED SIMULATORS

### **ALDEC CADENCE MENTOR SYNOPSYS**

### SAS COMPLIANCE SUITE

Developed by PerfectVIPs to thoroughly exercise SAS designs, the compliance suite is a comprehensive verification test suite that provides hundreds of test cases.

- Verifies all layers of SAS designs
- Provides comprehensive design coverage targeted at Phy, Link, Transport, Port & Application layers
- Identifies all protocol violations
- Provides directed and constrained random regression testing capability
- Developed with actual customer designs

### SAS SOLUTIONS

Developed by PerfectVIPs to address different system level SAS architectures, the following SAS solutions are available.

# Verification IP:

- SAS Initiator VIP
- SAS Target VIP
- SAS Initiator/Target VIP
- SAS Expander VIP

# Compliance Suites:

- Initiator Compliance Test Suite
- Target Compliance Test Suite